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Auto-Scale Factor algorithm for MIMO channel hardware simulator: Toward higher and stable SNR

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ABSTRACT

A hardware simulator facilitates the test and validation cycles by replicating channel artefacts in a controllable and repeatable laboratory environment. In this paper, a new Auto-Scale Factor (ASF) based architecture of the digital block of the hardware simulator for MIMO radio propagation channel is introduced. A detailed study shows that this architecture increases the Signal-to-Noise Ratio (SNR) of the output signals when the input signals or the impulse responses of the channel (h) are attenuated. The architecture is implemented on a Xilinx Virtex-IV FPGA. the occupation on the FPGA and the accuracy of this architecture are analyzed.

CONCLUSION

To decrease the error at the output of the hardware simulator, an ASF-based architecture is used. A detailed study shows that for high attenuation of the impulse responses and the input signal, the SNR of the output signals increases significantly. The average global SNR is increased by 37 dB for ± 7 dB variation of h in time. Moreover, it can attend 100 dB for an attenuation up to 15 dB of the impulse responses. Simulations will be made using a Virtex-VII [1] platform will allow us to simulate up to 8×8 MIMO channels and higher. A graphical user interface will be designed to allow the user to reconfigure the channel parameters. Also, cognitive hardware simulator for heterogeneous environments will be realized.

I. INTRODUCTION

The architecture of the digital block of the hardware simulator is mapped onto a Field Programmable Gate Array (FPGA) Virtex-IV [1] that has a great flexibility in algorithm design [2]. The channel models can be obtained from standard models, as the TGN 802.11n [3] and the 3GPP-LTE models [4], or from measurements conducted with the MIMO channel sounder designed and realized at IETR [5]. In the MIMO context, little experimental results have been obtained regarding time-variations, partly due to several limitations of the channel sounding equipment [6]. However, theoretical models of time-varying channels can be obtained using Rayleigh fading and Kronecker correlation-based model [7].

At IETR, several architectures of the digital block of a hardware simulator have been studied [8]. Typically, radio propagation channels are simulated using Finite Impulse Response (FIR) filters, as in [8, 9]. The Fast Fourier Transform (FFT) modules with algebraic product can also be used, as in [8, 10]. However, these considered frequency architectures operate correctly for signals not exceeding the FFT size. Thus, new frequency architecture avoiding this limitation has been presented and tested [11, 12]. Moreover, [12, 13] show that the time domain architecture is better in terms of occupation on FPGA, output error and latency.

In this paper, an improved time domain architecture based on an ASF (Auto-Scale Factor) is proposed. The main contribution of this architecture is presented as follow:

- To decrease the error at the simulator output signals, it is better to consider a large number of bits in the architecture for the input signal x and for h . In the context of mobile radio, x and h cannot be predicted and they can undergo fading and be strongly attenuated. If the signal is low, it will not be quantified on a sufficient number of bits. Thus, the error of the output signals of the channel simulator will increase widely. The proposed solution consists on multiplying x and h by an ASF (Auto-Scale Factor) that increases the output signals and makes it possible to quantify them on a higher number of bits in order to decrease the error at the output. Moreover, the received signal is divided by the correct ASF to obtain the correct output.
- Some MIMO hardware simulators are proposed by industrial companies. The leader of hardware channel simulators are Spirent [14] and Elektrobit (Propsim F32) [15]. These simulators are standalone units that provide the fading output signal/signals for SISO/MIMO systems in the form of digital samples. However, they present an accuracy of ± 1 dB at the output signals [13, 14]. With the ASF-based architecture the error of the output signals of the simulator is decreased and the accuracy is improved to ± 0.000155 dB. Moreover, the industrial hardware simulators may not offer to the user enough

flexibility when configuring the wireless channel parameters to test the system under different environmental conditions. A low cost channel simulator, as presented in this paper, is therefore required to provide the user the flexibility to measure the performance of the wireless system under real environmental conditions.

II. CHANNEL DESCRIPTION

The well known TGN channel residential model B [3] is used for the test with WLAN 802.11ac signals. To obtain a time-variant channel, Rayleigh fading method with the Kronecker correlation-based model is used [7]. For an environmental speed of 1.2 km/h and a central frequency of 5 GHz, the Doppler frequency f_d is 6 Hz and the refresh frequency $f_{ref} = 15$ Hz between two successive profiles.

The new architecture is tested with 10000 successive profiles (which enable the simulation on 11 minutes) of time-varying channel.

III. ASF-BASED DIGITAL BLOCK ARCHITECTURE DESIGN

The new 2x2 MIMO ASF-based architecture is presented in Fig 1. The two signals $x_1(t)$ and $x_2(t)$ are the input signals of the 2x2 MIMO channel, and the two signals $y_1(t)$ and $y_2(t)$ are the output signals.

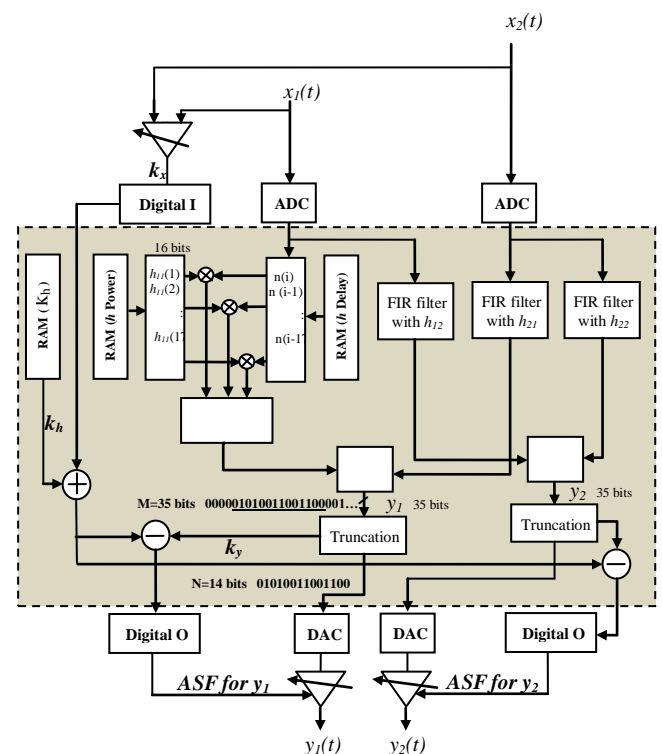


Fig. 1. Principle scheme using ASF.

The coloured large block is the programmable digital part (Virtex-IV) of the hardware simulator. "I" stands for Input and "O" for Output.

The maximum voltage supported by the Analogue-Digital Convertor (ADC) is 1 V. If $x_1 < 0.25$ V, it is multiplied by where is the integer verifying:

$$- \quad (1)$$

$$\text{with} \quad - \quad (2)$$

where is the smallest integer greater than (or equal to) .

In the same way, If $x_2 < 0.25$ V, it is multiplied by where is the integer verifying:

$$- \quad (3)$$

$$\text{with} \quad - \quad (4)$$

The input signal cannot exceed 1 V. Thus, we define by: (5)

In fact, we cannot provide the digital input by and because the ASF calculated and provided to the digital output will be unknown.

If $h_{max} = \max(|h|) < 0.5$, it is be multiplied by where:

$$- \quad (6)$$

$$\text{and} \quad - \quad (7)$$

is determined for every MIMO profile and it is saved in a RAM block in the FPGA. A gain controlled amplifier is placed before the ADC to control and send it to the FPGA. Also, controlling the power of x at a sampling period smaller than the sampling period of the FPGA is not easy. Thus, is provided for a package of x samples.

In the case of a brutal truncation, $ASF_{bth} =$, and using just the ASF on h , $ASF_{bh} =$. Moreover, a better solution is the sliding truncation (used in Figure 1) that selects the most significant bits. This truncation scans the bits until it detects a "1" bit, then it considers the 14 bits just form the first "0" bit that stands before it. In fact the ADC and the Digital-Analogue convertor (DAC) have a resolution of 14 bits. In this case, if the output signals are presented on more than 14 bits, the sliding factor has to be considered to obtain the correct output signal. Thus, $ASF =$, and using just the ASF on h , $ASF_{sh} =$. The resulting ASF is

sent to a gain controlled amplifier to restore the true value of the output signals, as presented in Figure 1.

The FPGA Virtex-IV has a limited number of digital outputs, thus the quantification of ASF is discussed in Section V.

IV. HARDWARE IMPLEMENTATION

Four FIR filters are used to implement a 2×2 MIMO channel. For TGN channel model B, each FIR filter has 9 DSP blocks (multipliers) which is equal to the number of taps of the impulse response. The Virtex-IV SX35 (described in [11]) prototyping board utilisation summary is given in Table I with the circuit used to reload the channel coefficients.

We have developed our own FIR filter instead of using Xilinx MAC filter to make it possible to reload the filter coefficients.

TABLE I. VIRTEX-IV UTILISATION FOR MIMO 2×2 ASF-BASED ARCHITECTURE

Logic Utilisation	Used	Available	Utilisation
Slice Flip Flops	1,615	30,720	5 %
4 input LUTs	2,556	30,720	8 %
Occupied Slices	2,090	15,360	13 %
Bonded IOBs	40	448	8 %
BUFG/BUFGCTRLs	1	32	3 %
FIFO16/RAMB16s	37	192	19 %
DSP48s	36	192	18 %

Figure 2 shows the connection between the computer and the FPGA board to reload the coefficients.

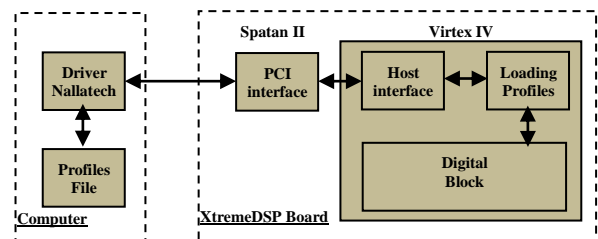
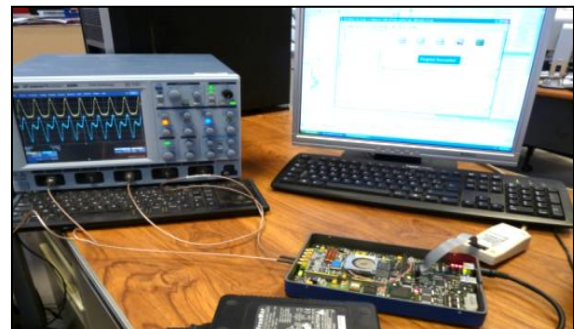


Fig. 2. Connection between the computer and the XtremeDSP board.

For the test, 10000 successive profiles of a 2x2 MIMO time-varying channel are considered. The refreshing frequency f_{ref} is chosen to be 15 Hz for $v = 1.2$ km/h. The refreshing period is $t_{ref} = 66.66$ ms during which we must refresh all of the four profiles, i.e. 9 taps \times 4 FIR filters = 36 words of 16 bits = 72 bytes to transmit a MIMO profile, which is $72/t_{ref} = 1.08$ kBps.

The PCI bus is chosen to load the profiles of the impulse responses. It has a speed of 30 MB/s. While a MIMO profile is used, the following MIMO profile is loaded and will be used after the refresh period.

The time domain architecture presented in [8] and [10] produces an occupation of 11 % to 13 % of slices on the FPGA for one SISO channel. However, the ASF-based architecture presents an occupation of 3 % for one SISO channel and 13 % for 2x2 MIMO channel.

V. ARCHITECTURE ACCURACY

In order to determine the accuracy, a comparison is made between theory/ Xilinx output signals. The input signals are considered the same for simplification: $x(t) = x_1(t) = x_2(t)$. x is considered Gaussian and it is quantified on 14 bits. It presents the two 2x2 MIMO channel inputs:

where $f_s = 165$ MHz is the sampling frequency, $T_s = 1/f_s$ is the sampling period, $W_t = 250T_s$, $m_x = 3 W_t/4$ and $m_y = m_x/4$. The ADC/DAC converters have a full scale of $[-V_m, V_m]$, with $V_m = 1$ V. We consider $x_m = V_m / 4 < V_m / 2$ to test the ASF-based architecture.

The theoretic output signals are:

To analyze the difference between the output signals, the relative error is computed for each output sample to by:

and the relative SNR by:

$$SNR = 20 \log_{10} \left(\frac{\text{Signal Power}}{\text{Noise Power}} \right)$$

Figure 3 presents a snapshot of the theory and the Xilinx output signals. y_{th1} , y_{th2} , y_{ASF1} and y_{ASF2} presents $y_1(t)$, $y_2(t)$, Xilinx output 1 using ASF and Xilinx output 2 using ASF, respectively.

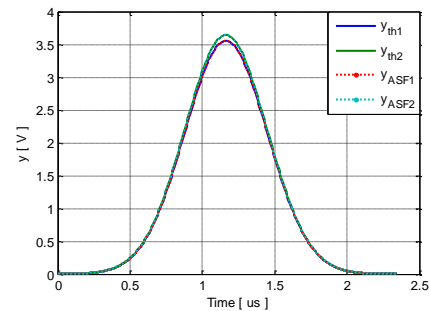


Fig. 3. Snapshot of the output signals.

Figure 4 presents the relative SNR without using ASF and using ASF of the snapshot taken in Figure 2. BT stands for Brutal Truncation and ST for Sliding window Truncation.

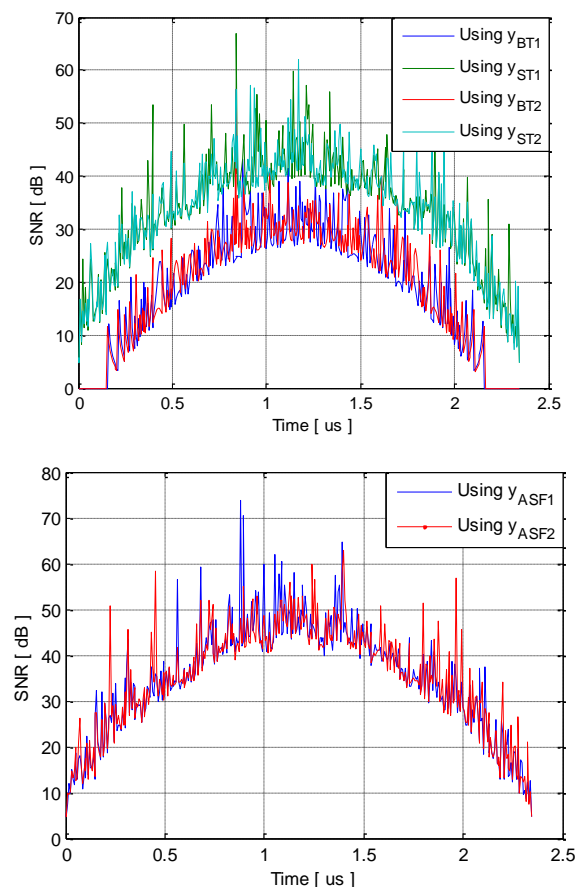


Fig. 4. Output relative SNR without using ASF (left) and using ASF (right).

Figure 4 shows the benefit of using ST. Moreover, using ASF provides a higher SNR. To present the results more clearly, the global values of the relative error and the SNR are necessary to evaluate the accuracy of the architectures. They are computed respectively by:

$$\text{Global SNR} = \frac{1}{N} \sum_{i=1}^N \text{SNR}_i \quad (13)$$

where $E = Y_{\text{Xilinx}} - Y_{\text{th}}$ is the error vector. The global SNR for all the MIMO profiles are presented in Fig 5.

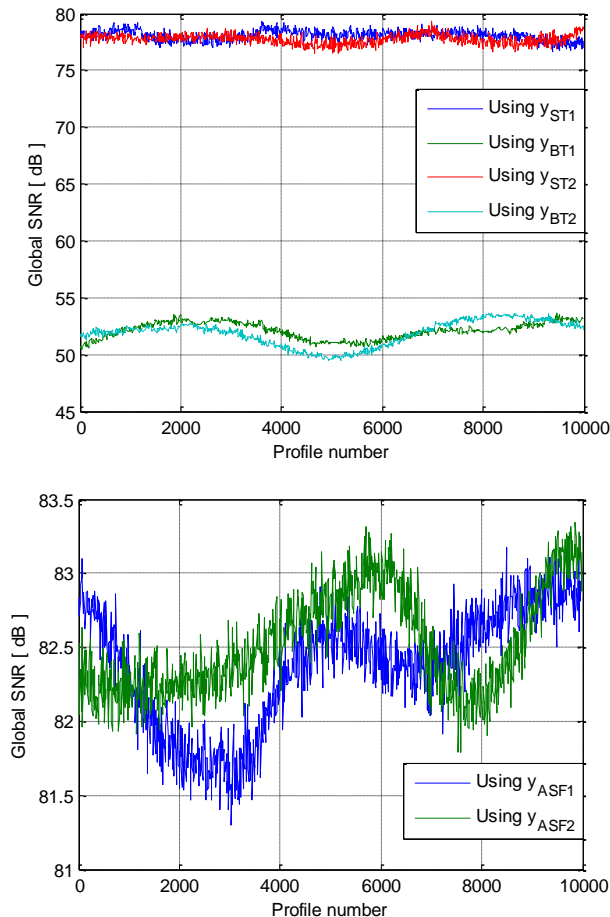


Fig. 5. Global relative SNR for all the MIMO profiles without using ASF (left) and using ASF (right).

In Fig 5, the BT provides a global SNR that ranges between 49 and 54 dB. The ST provides a higher global SNR that ranges between 77 and 79 dB. However, using the ASF-based architecture, the global SNR ranges between 81 and 84 dB.

These values depend on the range of the attenuation of h that varies in time. In our case, it varies between ± 7 dB. In fact, the ASF-based architecture has more benefit if the attenuation of h increases.

Therefore, Fig 6 presents the effect of the ASF on the global output SNR versus the attenuation of h . Moreover, it

presents the variation of the parameters k_{y_1} and k_{y_2} versus the attenuation of h .

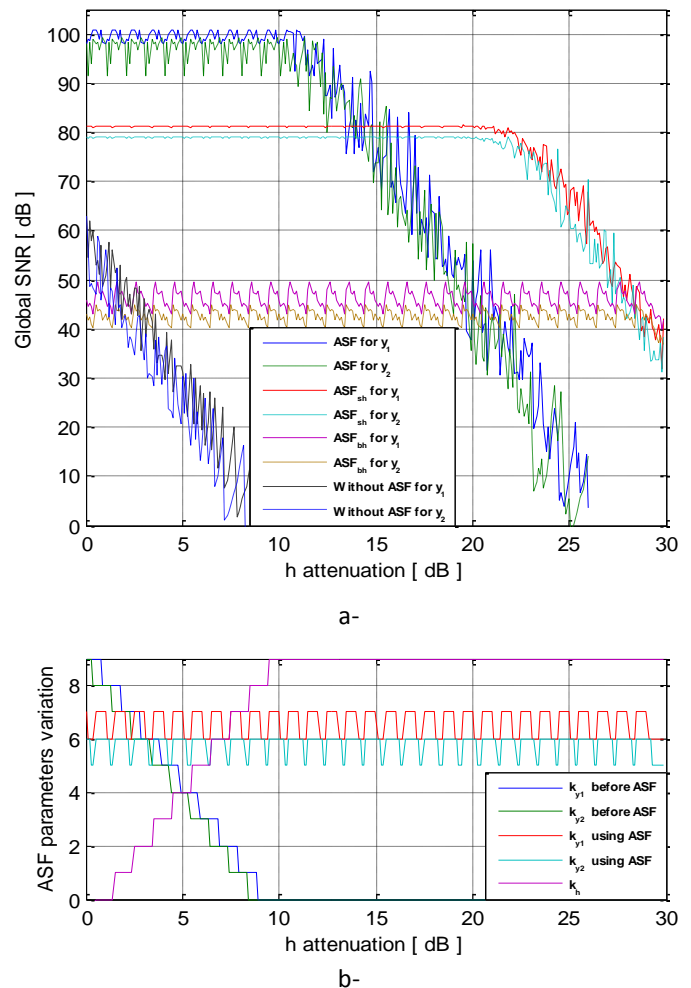


Fig. 6. ASF effects versus the attenuation of h : a- The global SNR, b- ASF parameters.

A FPGA Virtex-IV provides 34 pin (external digital I/O) Adjacent Bus Header on the motherboard of the FPGA. This will provides 28 direct bi-directional connections to the main user FPGA. The remainder of the pins are No-Connects (NC) pins. Thus, k_h provided to the input of the FPGA and the two ASF provided to the output y_1 and y_2 are quantified on 9 bits. For high attenuation, the ASF increase the global SNR significantly. For $ASF_{sh} = 18$, it will be quantified on 18 bits instead of 9. In fact, in this case, the 9 bits specified for k_h can be used. Thus, as shown in Fig 6, for an attenuation of h higher than 15 dB, it is better to eliminate k_h to obtain a higher and more stable output SNR. However, for an attenuation of h lower than 15 dB, it is better to use k_h and attend an SNR of 100 dB. Also, the result shows the benefit of the sliding truncation (ASF_{sh}) on the brutal truncation (ASF_{bh}).

Table 2 shows the error/SNR mean global values for all profiles using ST or BT with the ASF-based architecture and with a simple time domain architecture (without ASF).

TABLE II. MEAN GLOBAL RELATIVE ERROR () AND SNR

		With ASF		Without ASF	
		(%)	(dB)	(%)	(dB)
y_1	ST	0.0072	83.01	0.0132	77.65
	BT	0.2661	51.67	0.4724	46.62
y_2	ST	0.0072	82.88	0.0130	77.79
	BT	0.2570	51.95	0.5064	46.01

The mean global SNR values show the benefit of using an ASF-based architecture. The SNR is increased by 5 dB compared to a time domain architecture using just ST, and by 37 dB compared to the simple time domain architecture using BT.

ACKNOWLEDGMENT

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